

quantumdata™ M42d DisplayPort 2.0 Video Analyzer/Generator

Full 80Gb/s Link Rate Functional and Compliance Tester



Key Features

- Equipped with both DP standard and USB-C ports for Tx and Rx functions
- Test DP sources 10Gb/s, 13.5Gb/s & 20Gb/s lane rates at the new 128b/132b line coding
- View incoming video and metadata—including DSC compressed—from a source device
- Capture and decode incoming video, protocol, control packets including Display Stream Compression (DSC)
- Video generator to test displays and monitors at UHBR lane rates with large format & image library
- Configure link training parameters to test display's handling of link training on video generator
- Generate Display Stream Compression (DSC), select patterns and configure slices and video parameters
- View and edit EDID and DPCD registers
- Monitor Aux Channel transactions while emulating a DP 1.4 or DP 2.0 source or sink
- Passively monitor the Main Link and Aux Channel between a source & display at all UHBR lane rates
- Run tests on source and **NEW!** sink devices with Panel Replay capability
- Support for LTTPR in non-transparent mode for 128b/132b at UHBR rates at 8b/10b line code for lane rates up to HBR3
- View Power Delivery (PD) protocol negotiations for USB-C DP Alt Mode
- **UPDATED!** DP 2.0 Link Layer compliance tests on source & sink devices up to 20.0Gb/s per lane
- **NEW TESTS!** DP 2.0 LTTPR compliance tests on source & sink devices up to 20.0Gb/s per lane
- **UPDATED!** DP Adaptive Sync compliance tests on source and sync devices
- **NEW!** Run DP Adaptive Sync functional tests on source and sync devices
- Run approved DP 1.4 Link Layer compliance tests on sources and sinks up to 8.1Gb/s per lane
- Run DP 1.4 Forward Error Correction (FEC) and Display Stream Compression (DSC) compliance tests for sources and sinks
- Run HDCP 2.2/3 compliance tests on DisplayPort sources, sinks and branch devices
- Run audio tests using LPCM sine wave audio tones
- Run Golden Frame PRN error tests on sources and in loopback configuration
- Run tests on embedded DisplayPort (eDP) 1.4b sources and panels (limited)
- **UPDATED!** Application Programming Interface (API) for automated testing for compliance & functional testing.

The Teledyne LeCroy quantumdata M42d Video Analyzer/Generator provides an unprecedented combination of functional and compliance testing for video, audio and protocol of DisplayPort 2.0 and DisplayPort 1.4. The M42d supports legacy DisplayPort lane rates of 1.62, 2.7, 5.4, 8.1 Gb/s and the new DP 2.0 higher speed lane rates and new line coding—128b/132b—of 10.0, 13.5 & 20.0Gb/s data rates up to 4 lanes. The protocol analyzer provides a snapshot status view and deep analysis using captures of incoming DisplayPort 2.0 (and DP 1.4) streams from source devices including DSC/FEC compressed streams. The M42d's video generator can be used for testing silicon development boards, displays, docking stations and hubs, USB-C adapters, extenders, etc. The video generator offers a large library of standard video timings and test patterns necessary for testing next generation high resolution displays.

The M42d supports a full suite of DP 1.4 link layer, forward error correction (FEC) and display stream compression (DSC) compliance tests for both sources and sinks. (Compliance tests for DP 2.0 are currently being implemented.)

The Passive Probe feature based on Teledyne LeCroy's cutting-edge T.A.P.4™ technology, enables full monitoring of the DisplayPort Main Link and the Aux Channel between two DisplayPort devices up to 20 Gb/s lane rates future.

Operation

The M42d supports generation and analysis of the DisplayPort data streams through the user-friendly ATP Manager. The M42d can be controlled through the ATP Manager operated either via a laptop connected to the M42d RJ45 LAN port or through a USB keyboard and mouse and a connected UHD HDMI admin display.

M42d Video Analyzer Generator



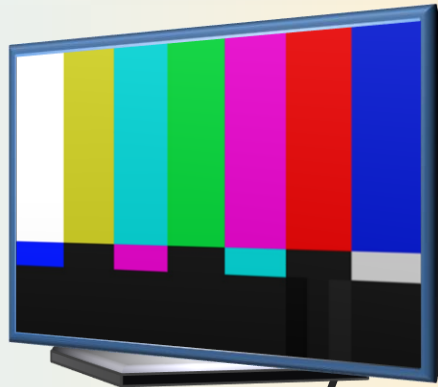
Keyboard & mouse for
 M42d ATP Manager
 Control

DISPLAY TESTS – VIDEO TESTING

Video Generation

The M42d supports video and audio functional testing at UHBR lane rates up on 1, 2 and 4 lanes to support high resolution formats. The M42d has an extensive set of video formats and library of test patterns. You can specify lane configurations for link training (below).

DP 2.0 Sink DUT



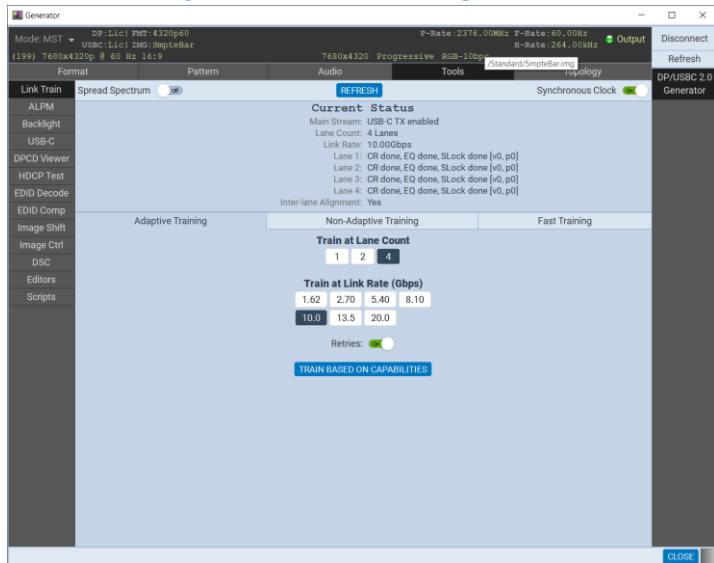
External Host PC for ATP Manager



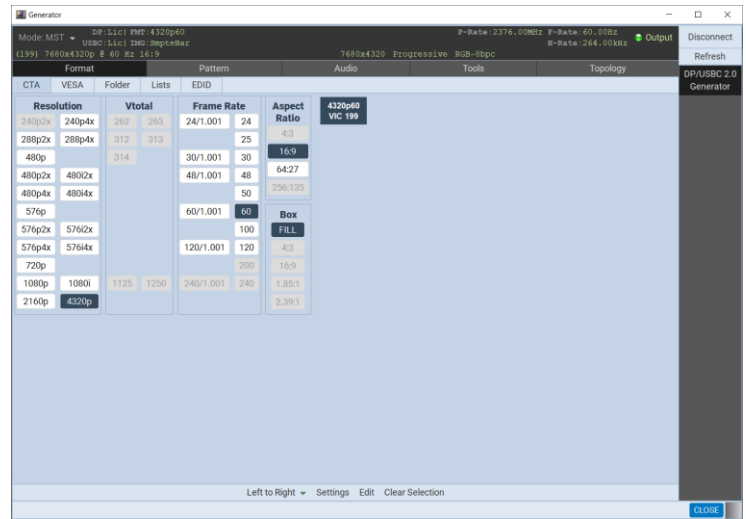
USB-Cable

Display (Sink) Test Setup

Link Training Control and Configuration



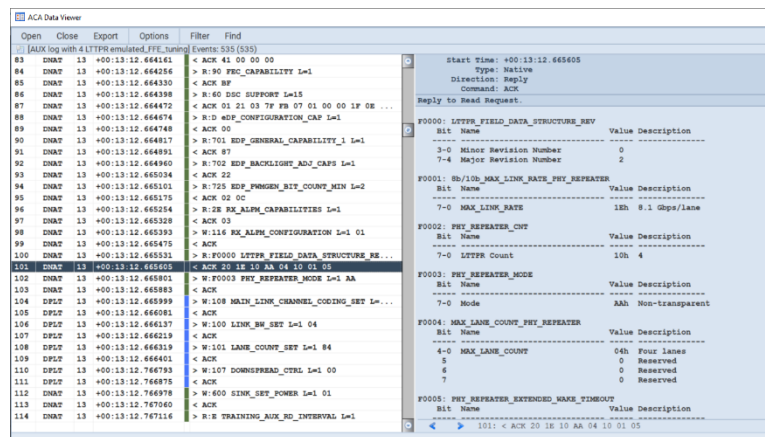
Format Selection



Aux Channel Analyzer (ACA)

The M42d's Auxiliary Channel Analyzer (ACA) feature enables you to monitor the DP Aux Channel for link training, MST negotiations, HDCP transactions, DP Alt Mode PD negotiations and EDID exchanges between the M42d Rx port and a connected source. The ACA logs these events and assigns precise timestamps to them. You can view the details of each transaction. These ACA logs can be saved and disseminated for further analysis by colleagues and other subject matter experts.

Aux Channel Analyzer



Link Training Control and Configuration

The M41d's link training control feature enables you to configure the link training parameters. You can set limits on the lane count and link rate and allow the link training engine to establish link training based on those limitations or you can force link training parameters—lane count, link rate, voltage swing, pre-emphasis.

SOURCE TESTS – VIDEO & PROTOCOL ANALYSIS

Receiver - Basic & Capture Analyzer

The M42d's Basic Analyzer enables you to view the incoming video, lanes and link rate, timing, colorimetry and various other metadata in real time at a glance. The Basic Analyzer mode provides a basic confidence test to verify that the incoming video is essentially correct. The Rx port emulates any EDID on to test a source devices handling of various EDIDs. You can also configure DPCD registers for emulating on the DP Rx port using the DPCD Editor.

Receiver – Basic Analysis



External Display for ATP Manager

DP 2.0 Source DUT

HDMI cable

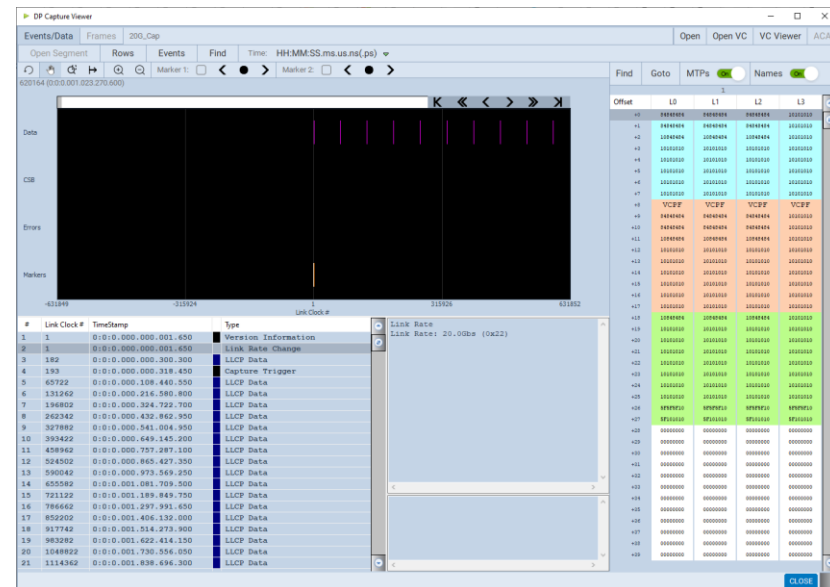
USB-Cable

Source Test Setup

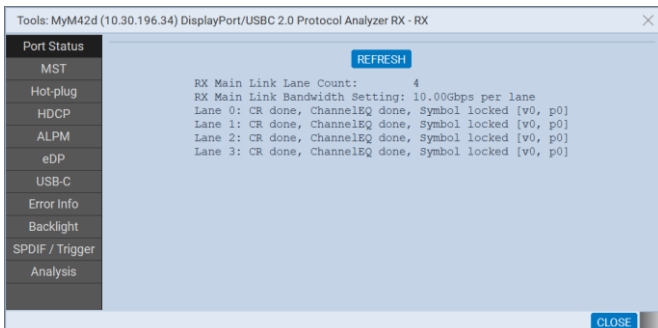
Receiver - Capture Analyzer

The deep Capture Analyzer enables you to view the protocol data of the high-speed link (shown below) and the underlying virtual channels (shown below). The Capture Analyzer provide deep insight into the data, control symbols, video, metadata and protocol data.

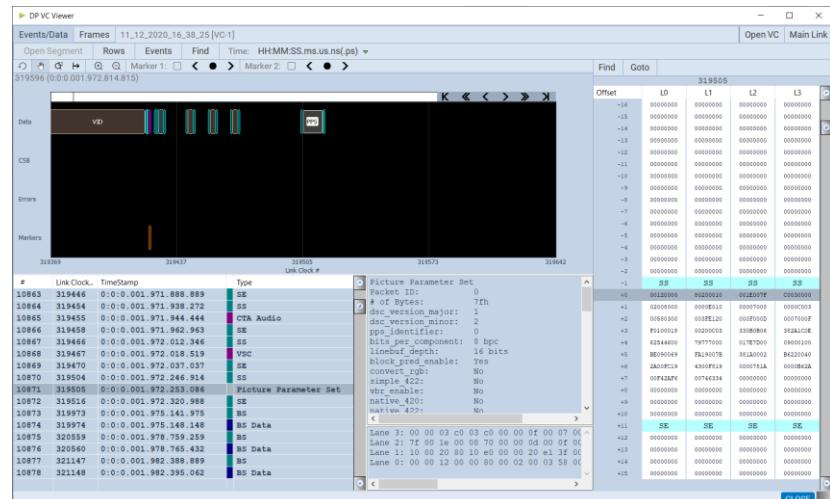
Capture Analysis (Main Link)



Link Training Status



Capture Analysis – Virtual Channels



DP 2.0/1.4 LINK LAYER SOURCE COMPLIANCE

Source Link Layer Compliance

The DP source link layer compliance are ideal for self-testing or pre-testing your HBR3 or UHBR-capable DisplayPort source product prior to submission to an Authorized Test Center for approval. Pre-testing provides added assurance that your product will pass at the ATC when submitted. The compliance tests enable you to view the captured data and detailed test results which help pinpoint the cause of compliance test failures. You can link to the aux channel traces in the Aux Channel Analyzer (ACA) to view the root cause of failures.

External Display for ATP Manager

DP 2.0 Source DUT

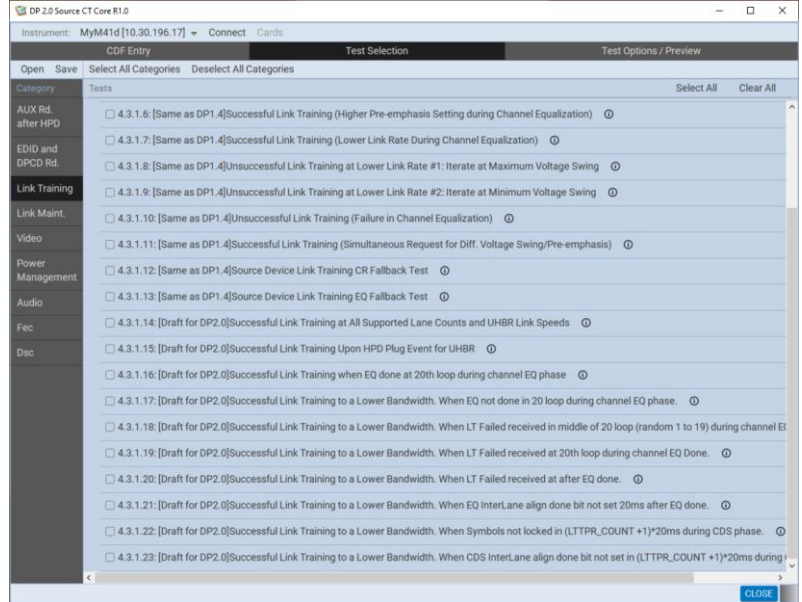
HDMI cable

USB-Cable

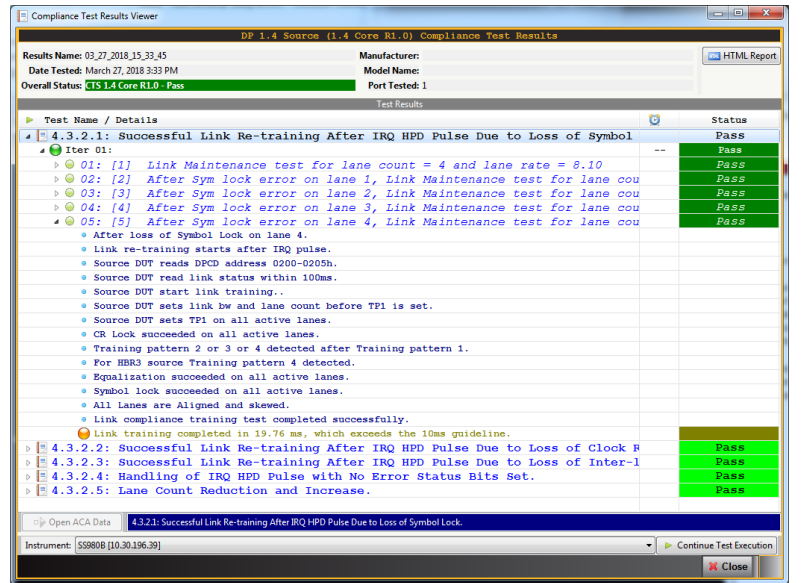
Source Test Setup



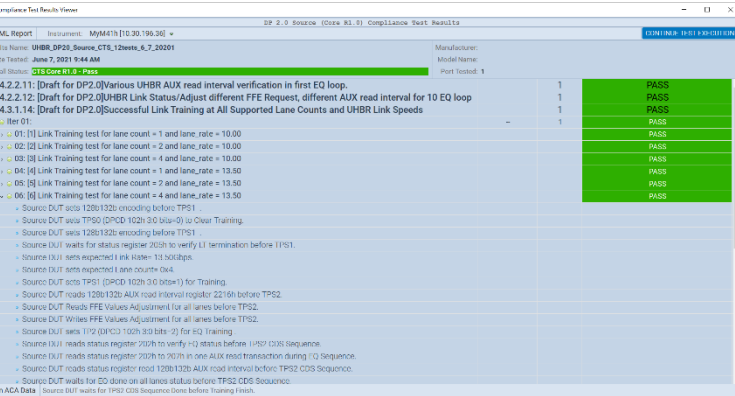
DP 1.4/2.0 Source Link Layer Compliance - Test Selection



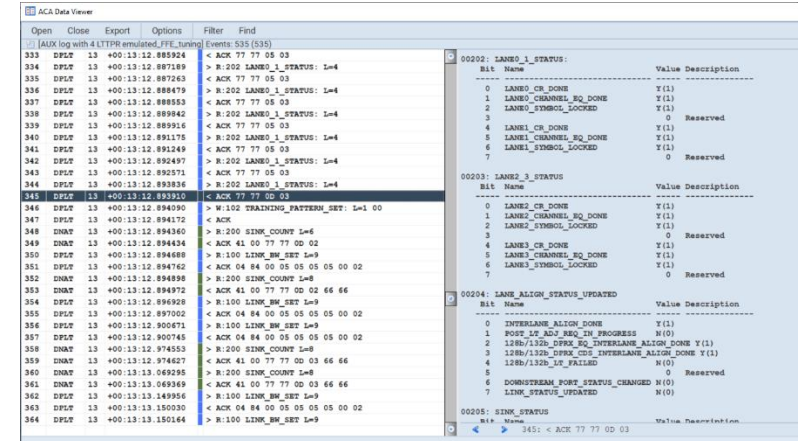
DP 1.4 Source Link Layer Compliance Test Results



DP 2.0 Source Link Layer Compliance Test Results



DP Aux Channel Traces – From LLC Test

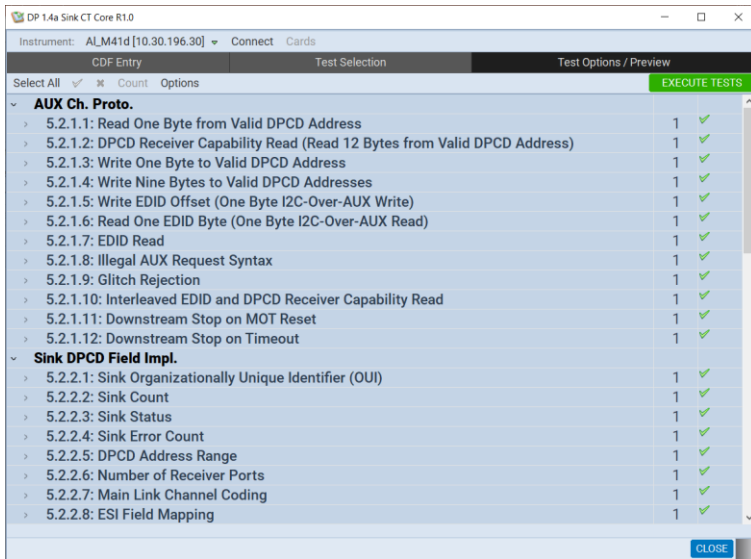


DP 2.0/1.4 LINK LAYER SINK COMPLIANCE

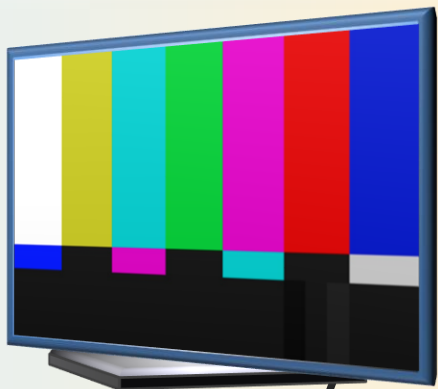
Sink Link Layer & EDID Compliance

The DP sink (display) and EDID/DisplayID and Link Layer compliance tests are ideal for pre-testing or self-testing (where permitted) your DisplayPort display product prior to submission to an Authorized Test Center for approval. Pre-testing provides added assurance that your product will pass at the ATC when submitted. The compliance tests (below right) enable you to view the captured data and detailed test results which help pinpoint the cause of compliance test failures. The link layer compliance test suite now includes tests for forward error correction (FEC). You can link to the aux channel traces in the Aux Channel Analyzer (ACA) to view the root cause of failures (below).

DP 1.4 Link Layer Compliance - Test Selection



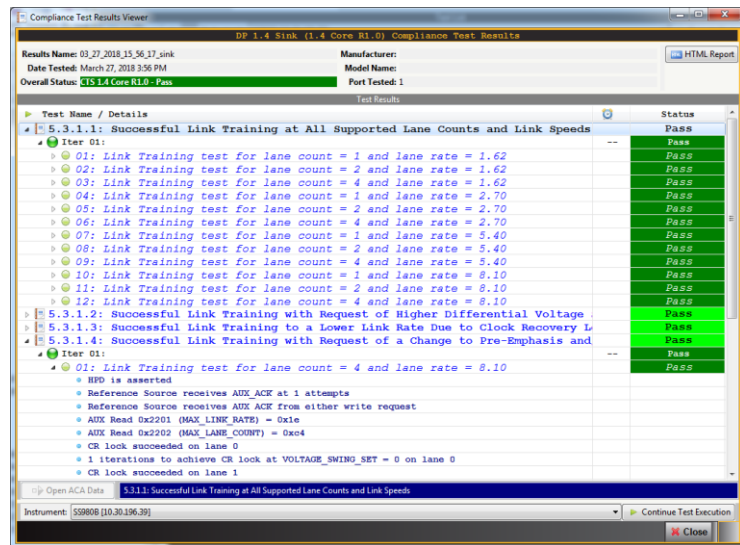
DP 2.0 Sink DUT



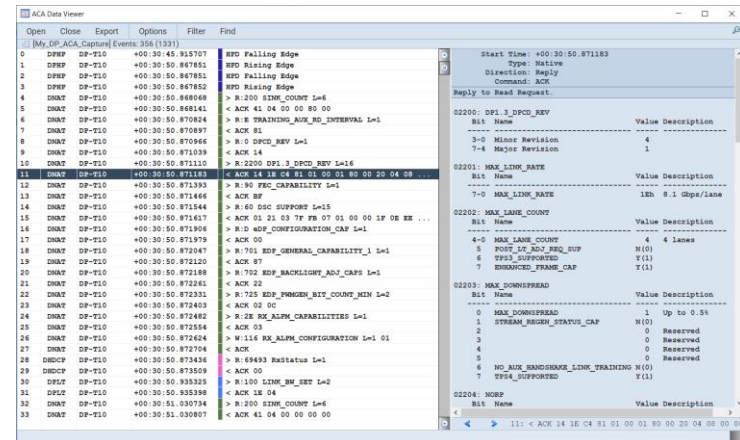
External Host PC for ATP Manager

USB-Cable

DP 1.4 Link Layer Compliance - Test Results



DP Aux Channel Traces – From LLC Test



Display (Sink) Test Setup

ADAPTIVE SYNC FUNCTIONAL TESTING

Adaptive Sync Source Functional Testing

The M42d now supports the testing of Adaptive Sync-capable source and sink devices for HBR3 rates. The Adaptive Sync analyzer for testing Adaptive Sync-capable source devices enables you to view the variations in the vertical blanking to lower the refresh rate. The Adaptive Sync video generation for testing Adaptive Sync-capable displays or monitors enables you to send different test patterns that increase and decrease the vertical blanking to increase or decrease the refresh rate of the display. Adaptive Sync testing for sink devices is currently only supported through the command line with GUI support to be provided in the future.

Adaptive Sync Capture Analysis

You can view the Adaptive Sync variations in the vertical blanking in the Capture Analyzer as shown below.

Adaptive Sync Aux Channel Analyzer (ACA)

You can view the Adaptive Sync discover and configuration transactions occurring over the Aux Channel with the Aux Channel Analyzer (ACA) as shown left.

The screenshot shows the ACA Data Viewer interface. The main window displays a list of events with columns for time, device type, and data. A detailed view of a specific event is shown on the right, including its bit name, value, and description.

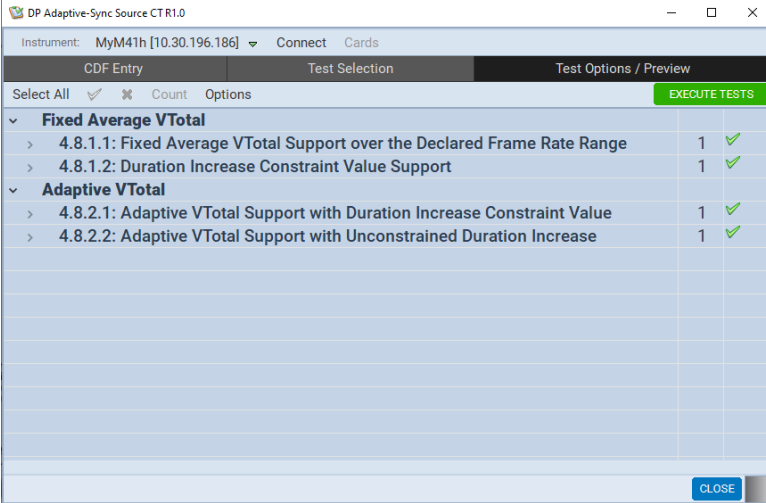
Time	Device	Data
256	DI2C DP-R12	> R:AD EDID L=16
257	DI2C DP-R12	< DEFE
258	DI2C DP-R12	> R:AD EDID L=16
259	DI2C DP-R12	< ACK 00 00 00 00 00 00 00 00 00 00 00 00 00 00 16 90
260	DPLT DP-R12	> R:100 LINK_BW_SET L=9
261	DPLT DP-R12	< ACK 1E 84 00 08 08 08 08 00 01
262	DPLT DP-R12	> R:100 LINK_BW_SET L=9
263	DPLT DP-R12	< ACK 1E 84 00 08 08 08 08 00 01
264	DNAT DP-R12	> R:2214 FEATURE_ENUMERATION_LIST_COUNT L=1
265	DNAT DP-R12	< ACK 03
266	DNAT DP-R12	> R:7 DOWN_STREAM_PORT_COUNT L=1
267	DNAT DP-R12	< ACK 44
268	DPLT DP-R12	> R:107 DOWNSPREAD_CTRL L=1
269	DPLT DP-R12	< ACK 00
270	DPLT DP-R12	> R:107 DOWNSPREAD_CTRL L=1 80
271	DPLT DP-R12	< ACK
272	DPLT DP-R12	> R:107 DOWNSPREAD_CTRL L=1
273	DPLT DP-R12	< ACK 80
274	DPLT DP-R12	> R:100 LINK_BW_SET L=9
275	DPLT DP-R12	< ACK 1E 84 00 08 08 08 08 00 01
276	DPLT DP-R12	> R:100 LINK_BW_SET L=9
277	DPLT DP-R12	< ACK 1E 84 00 08 08 08 08 00 01
278	DPFP DP-R12	HPO Falling Edge
279	DPFP DP-R12	HPO Rising Edge
280	DNAT DP-R12	> R:200 SINK_COUNT L=6
281	DNAT DP-R12	< ACK 41 00 22 22 81 00
282	DNAT DP-R12	> R:1E TRAINING_AUX_RD_INTERVAL L=1
283	DNAT DP-R12	< ACK 81
284	DNAT DP-R12	> R:10 DPCD_SERV L=1
285	DNAT DP-R12	< ACK 14
286	DNAT DP-R12	> R:2200 DPCD_3_DPCD_SERV L=14
287	DNAT DP-R12	< ACK 14 1E C4 80 01 00 01 40 00 20 04 08 00 00 81 00
288	DNAT DP-R12	> R:2210 DPCD_FEATURE_ENUMERATION_LIST L=16
289	DNAT DP-R12	< ACK 0A 00 00 00 03 00 85 00 00 00 00 00 00 00 00
290	DNAT DP-R12	> R:90 FEC_CAPABILITY L=1
291	DNAT DP-R12	< ACK BE
292	DNAT DP-R12	> R:160 DPC SUPPORT L=16
293	DNAT DP-R12	< ACK 00 21 03 7F EB 07 01 00 00 1F 0E EE 08 07 00 00
294	DNAT DP-R12	> R:1D eDP_CONFIGURATION_CAP L=1
295	DNAT DP-R12	< ACK 00
296	DNAT DP-R12	> R:701 eDP_GENERAL_CAPABILITY_1 L=1
297	DNAT DP-R12	< ACK 87

The screenshot shows the DP Capture Viewer interface. The main window displays a waveform with various data streams (Data, CSB, Errors, Markers) over time. A detailed view of an Adaptive-Sync event is shown in the bottom right, including its packet ID, version, and valid data count.

#	Link Clock #	TimeStamp	Type
1	1	0:0:0.000.000.001.235	Version Information
2	1	0:0:0.000.000.001.235	Link Rate Change
3	4	0:0:0.000.000.004.938	Fill
4	23	0:0:0.000.000.028.395	BS
5	24	0:0:0.000.000.029.630	BP
6	25	0:0:0.000.000.030.864	BP
7	26	0:0:0.000.000.032.099	BS
8	27	0:0:0.000.000.033.333	BS Data
9	27	0:0:0.000.000.033.333	Start of Frame
10	37	0:0:0.000.000.045.679	Capture Trigger
11	41	0:0:0.000.000.050.617	SS
12	42	0:0:0.000.000.051.852	SS
13	43	0:0:0.000.000.053.086	MSA
14	52	0:0:0.000.000.064.197	SE
15	228	0:0:0.000.000.281.481	SS
16	229	0:0:0.000.000.282.716	Audio TimeStamp
17	241	0:0:0.000.000.297.531	SE
18	360	0:0:0.000.000.444.444	SS
19	361	0:0:0.000.000.445.679	CTA Audio

ADAPTIVE SYNC COMPLIANCE TESTS

Adaptive Sync Source Compliance Test Selection



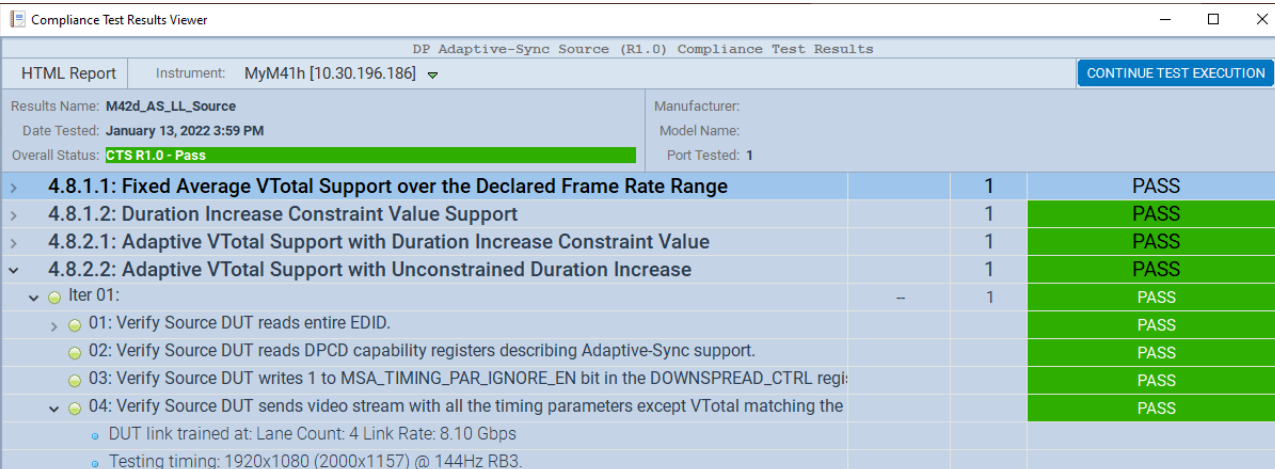
Adaptive Sync Sink Compliance Test Selection



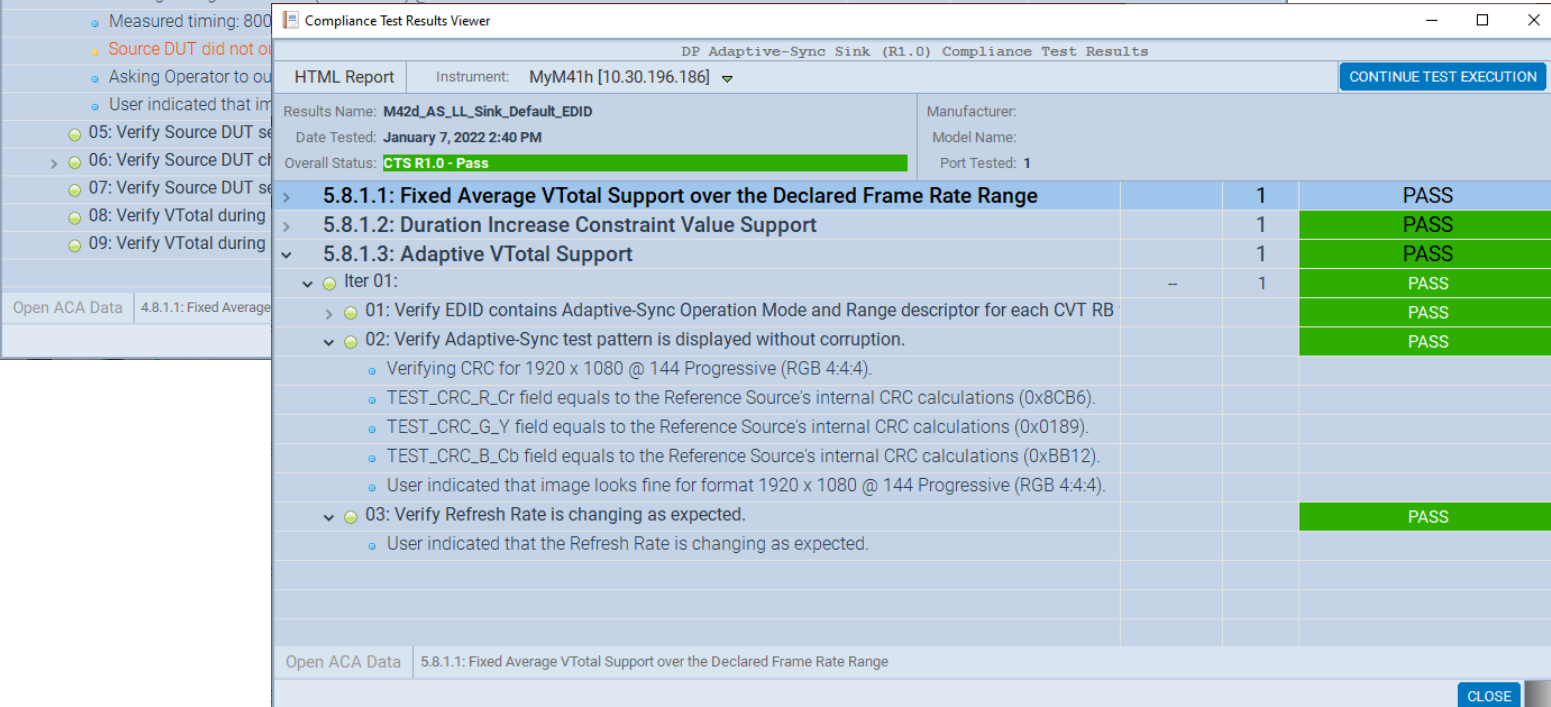
Adaptive Sync Compliance Testing

The M42d supports Adaptive Sync compliance testing for both source and sink devices. The examples below (source left, sink right) show the details provided with the compliance test results. Currently tests are provided for rates up to HBR3 with UHBR support coming in a future release.

Adaptive Sync Source Compliance Test Results



Adaptive Sync Sink Test Results

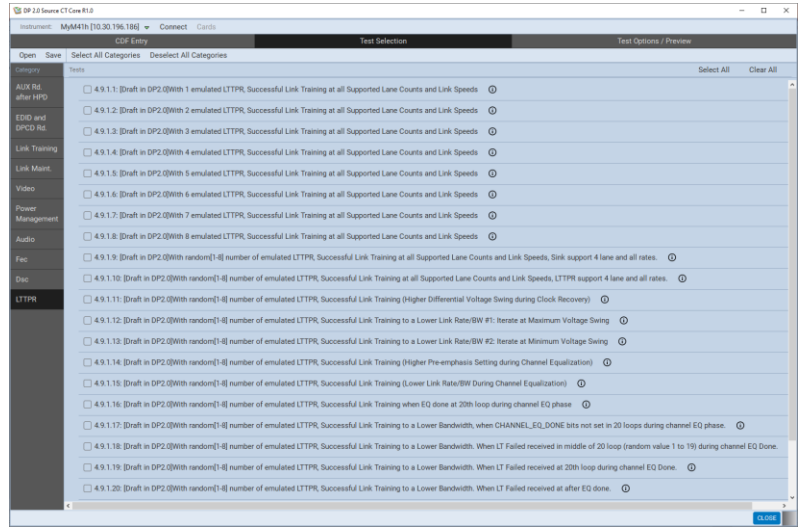


DP 2.0 LTTTPR SOURCE COMPLIANCE

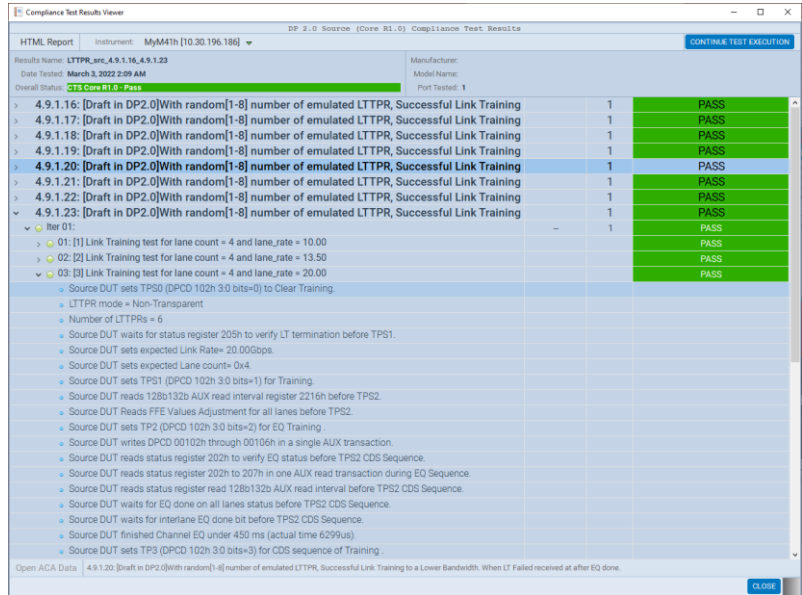
LTTTPR-Capable Source Compliance

The DP Source Link Training Tunable Phy Repeater (LTTTPR) compliance are ideal for self-testing or pre-testing your HBR3 or UHBR-capable DisplayPort source product prior to submission to an Authorized Test Center for approval. Pre-testing provides added assurance that your product will pass at the ATC when submitted. The compliance tests enable you to view the captured data and detailed test results which help pinpoint the cause of compliance test failures. You can link to the aux channel traces in the Aux Channel Analyzer (ACA) to view the root cause of failures.

DP 2.0 Source LTTTPR Compliance - Test Selection



DP 2.0 Source LTTTPR Compliance Test Results



External Display for ATP Manager

DP 2.0 LTTTPR-Capable Source DUT

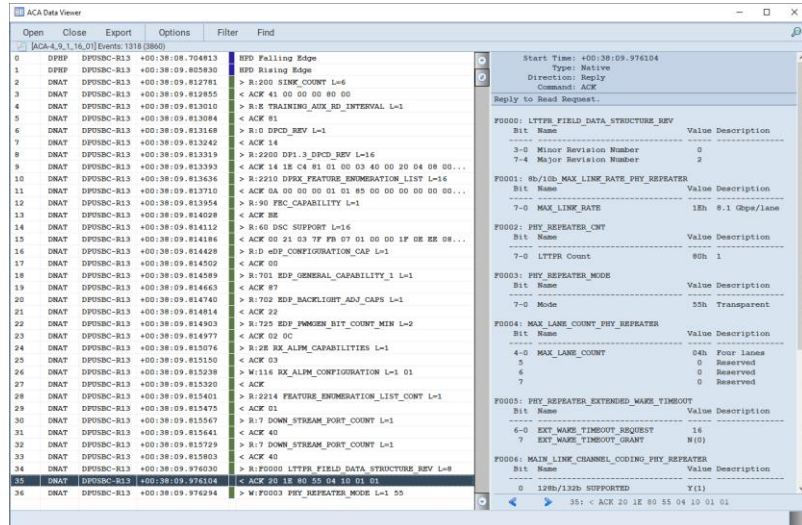


HDMI cable

USB-Cable

Source Test Setup

DP Aux Channel Traces – From LTTTPR Test



DP 2.0 LTPR SINK/DEVICE COMPLIANCE

LTPR-Capable Sink & LTPR Device Compliance

The DP Sink and Device Link Training Tunable Phy Repeater (LTPR) compliance are ideal for self-testing or pre-testing your HBR3 or UHBR-capable DisplayPort source product prior to submission to an Authorized Test Center for approval. Pre-testing provides added assurance that your product will pass at the ATC when submitted. The compliance tests enable you to view the captured data and detailed test results which help pinpoint the cause of compliance test failures. You can link to the aux channel traces in the Aux Channel Analyzer (ACA) to view the root cause of failures.

DP 2.0 LTPR Device Compliance - Test Selection

Compliance Test Results Viewer
DP 2.0 Sink (Core R1.0) Compliance Test Results

HTML Report Instrument: MyM41h [10.30.196.186] CONTINUE TEST EXECUTION

Results Name: LTPR_5.9.1.13_to_5.9.1.15
Date Tested: March 14, 2022 3:35 PM
Manufacturer: Model Name: Port Tested: 1

Overall Status: CTS Core R1.0 - Pass

- 01: Link Training test for lane count = 4 and lane_rate = 20.00
 - HPD is asserted
 - LTPR reports correct structure revision (DPDC F0000h = 0x20)
 - LTPR capability supports the link rate and lane count currently under test
 - Reference Source receives AUX_ACK at 1 attempts
 - Reference Source receives AUX_ACK from either write request
 - Sink DUT Capability supports UHBR RATE = 20.0 Gbps and MAX_LANE_COUNT = 4
 - Reference Source sets TP50 (DPDC 102h 3 0 bits=0) to Clear Training
 - INTRAHOP_AUX_REPLY_INDICATION bit clears before the 180ms timer expired.
 - Reference Source sets 128b132b encoding before TP51
 - Reference Source sets Link Rate = 20.00Gbps
 - Reference Source sets Lane count= 0x4
 - Reference Source sets LTPR Non-Transparent Mode (0xAA)
 - Reference Source sets TP51 (DPDC 102h 3 0 bits=1) for Training
 - Sink DUT reports 128b132b AUX read interval=6 secs (DPDC 2216h) before TP52
 - Sink DUT reports FFE Values(lane0, lane1, lane2, lane3) Adjustments for all lanes before 128b132b_DP_LT_FAILED bit (DPDC 204h bit 4) is NOT set before EQ loop
 - 128b132b_DP_DPRX_EQ_INTERLANE_ALIGN_DONE bit (DPDC 204h bit 2) is NOT set before EQ
 - 128b132b_DP_DPRX_CDS_INTERLANE_ALIGN_DONE bit (DPDC 204h bit 3) is NOT set before EQ
 - INTRAHOP_AUX_REPLY_INDICATION bit is clear
 - Reference Source sets TP2 (DPDC 102h 3 0 bits=2) for EQ Training
 - Sink DUT reports EQ done Status, Symbol lock Status (lane1,0), (lane2,1,0), (lane3,2,0,1)
 - Interlane CDS is not locked, as expected, before TP50
 - Reference Source reads the same lane status 250 times before setting TP50
 - Sink DUT sets the LT_Failed bit (DPDC 204h bit 4+1) and the Reference Source sets TP50 (DPDC 102h 3 0 bits=0) to Clear Training
 - INTRAHOP_AUX_REPLY_INDICATION bit clears before the 180ms timer expired.
 - Reference Source sets 128b132b encoding before TP51
 - Reference Source reduces the bandwidth after link training failed (Lane Count = 4, Link Rate = 1)
 - Reference Source sets TP51 (DPDC 102h 3 0 bits=1) for Training
 - Sink DUT reports 128b132b AUX read interval=6 secs (DPDC 2216h) before TP52

Open ACA Data 5.9.1.13: [Draft in DP2.0] LTPR 128b132b non-transparent successful Link Training to Lower Link Rate, due to failure in EQ Phase of UHBR.

DP 2.0 LTPR Sink Compliance - Test Selection

DP 2.0 LTPR Sink Compliance - Test Selection

Instrument: MyM41h [10.30.196.186] Connect Cards

Test Selection Test Options / Preview EXECUTE TESTS

- 4.9.1.1: [Draft in DP2.0] With 1 emulated LTPR, Successful Link Training at all Supported Lane Counts and Link Speeds 1 ✓
- 4.9.1.2: [Draft in DP2.0] With 2 emulated LTPR, Successful Link Training at all Supported Lane Counts and Link Speeds 1 ✓
- 4.9.1.3: [Draft in DP2.0] With 3 emulated LTPR, Successful Link Training at all Supported Lane Counts and Link Speeds 1 ✓
- 4.9.1.4: [Draft in DP2.0] With 4 emulated LTPR, Successful Link Training at all Supported Lane Counts and Link Speeds 1 ✓
- 4.9.1.5: [Draft in DP2.0] With 5 emulated LTPR, Successful Link Training at all Supported Lane Counts and Link Speeds 1 ✓
- 4.9.1.6: [Draft in DP2.0] With 6 emulated LTPR, Successful Link Training at all Supported Lane Counts and Link Speeds 1 ✓
- 4.9.1.7: [Draft in DP2.0] With 7 emulated LTPR, Successful Link Training at all Supported Lane Counts and Link Speeds 1 ✓
- 4.9.1.8: [Draft in DP2.0] With 8 emulated LTPR, Successful Link Training at all Supported Lane Counts and Link Speeds 1 ✓
- 4.9.1.9: [Draft in DP2.0] With random [1-8] number of emulated LTPR, Successful Link Training at all Supported Lane Cc 1 ✓
- 4.9.1.10: [Draft in DP2.0] With random [1-8] number of emulated LTPR, Successful Link Training at all Supported Lane C 1 ✓
- 4.9.1.11: [Draft in DP2.0] With random [1-8] number of emulated LTPR, Successful Link Training (Higher Differential Vo 1 ✓
- 4.9.1.12: [Draft in DP2.0] With random [1-8] number of emulated LTPR, Successful Link Training to a Lower Link Rate/V 1 ✓
- 4.9.1.13: [Draft in DP2.0] With random [1-8] number of emulated LTPR, Successful Link Training to a Lower Link Rate/B 1 ✓
- 4.9.1.14: [Draft in DP2.0] With random [1-8] number of emulated LTPR, Successful Link Training (Higher Pre-emphasis 1 ✓
- 4.9.1.15: [Draft in DP2.0] With random [1-8] number of emulated LTPR, Successful Link Training (Lower Link Rate/BW C 1 ✓
- 4.9.1.16: [Draft in DP2.0] With random [1-8] number of emulated LTPR, Successful Link Training when EQ done at 20th 1 ✓
- 4.9.1.17: [Draft in DP2.0] With random [1-8] number of emulated LTPR, Successful Link Training to a Lower Bandwidth, 1 ✓
- 4.9.1.18: [Draft in DP2.0] With random [1-8] number of emulated LTPR, Successful Link Training to a Lower Bandwidth, 1 ✓
- 4.9.1.19: [Draft in DP2.0] With random [1-8] number of emulated LTPR, Successful Link Training to a Lower Bandwidth, 1 ✓
- 4.9.1.20: [Draft in DP2.0] With random [1-8] number of emulated LTPR, Successful Link Training to a Lower Bandwidth, 1 ✓
- 4.9.1.21: [Draft in DP2.0] With random [1-8] number of emulated LTPR, Successful Link Training to a Lower Bandwidth, 1 ✓
- 4.9.1.22: [Draft in DP2.0] With random [1-8] number of emulated LTPR, Successful Link Training to a Lower Bandwidth, 1 ✓
- 4.9.1.23: [Draft in DP2.0] With random [1-8] number of emulated LTPR, Successful Link Training to a Lower Bandwidth, 1 ✓

DP 2.0 LTPR Device Compliance - Test Results

DP 2.0 LTPR Device Compliance - Test Results

Instrument: MyM41h [10.30.196.186] Connect Cards

Test Selection Test Options / Preview EXECUTE TESTS

- Capability
 - 7.1.1.1: [Draft in DP2.0] Data structure revision validation 1 ✓
 - 7.1.1.2: [Draft in DP2.0] Phy repeater count validation 1 ✓
 - 7.1.1.3: [Draft in DP2.0] Phy repeater lane count validation 1 ✓
 - 7.1.1.4: [Draft in DP2.0] Phy repeater link rate validation 1 ✓
 - 7.1.1.5: [Draft in DP2.0] Phy repeaters DPDC register validation at various LTPR position. 1 ✓
 - 7.1.1.6: [Draft in DP2.0] Phy repeater AUX read/write time budget validation 1 ✓
- 8b10b-Transparent
 - 7.1.2.1: [Draft in DP2.0] With 0 emulated LTPR, Successful Link Training at all Supported Lane Counts and 8b10b Link 1 ✓
 - 7.1.2.2: [Draft in DP2.0] With 1 emulated LTPR, Successful Link Training at all Supported Lane Counts and 8b10b Link 1 ✓
 - 7.1.2.3: [Draft in DP2.0] With 2 emulated LTPR, Successful Link Training at all Supported Lane Counts and 8b10b Link 1 ✓
 - 7.1.2.4: [Draft in DP2.0] With 3 emulated LTPR, Successful Link Training at all Supported Lane Counts and 8b10b Link 1 ✓
 - 7.1.2.5: [Draft in DP2.0] With 4 emulated LTPR, Successful Link Training at all Supported Lane Counts and 8b10b Link 1 ✓
 - 7.1.2.6: [Draft in DP2.0] With 5 emulated LTPR, Successful Link Training at all Supported Lane Counts and 8b10b Link 1 ✓
 - 7.1.2.7: [Draft in DP2.0] With 6 emulated LTPR, Successful Link Training at all Supported Lane Counts and 8b10b Link 1 ✓
 - 7.1.2.8: [Draft in DP2.0] With 7 emulated LTPR, Successful Link Training at all Supported Lane Counts and 8b10b Link 1 ✓
- 8b10b-Non-Transparent
 - 7.1.3.1: [Draft in DP2.0] With 0 emulated LTPR, Successful Link Training at all Supported Lane Counts and 8b10b Link 1 ✓
 - 7.1.3.2: [Draft in DP2.0] With 1 emulated LTPR, Successful Link Training at all Supported Lane Counts and 8b10b Link 1 ✓
 - 7.1.3.3: [Draft in DP2.0] With 2 emulated LTPR, Successful Link Training at all Supported Lane Counts and 8b10b Link 1 ✓
 - 7.1.3.4: [Draft in DP2.0] With 3 emulated LTPR, Successful Link Training at all Supported Lane Counts and 8b10b Link 1 ✓
 - 7.1.3.5: [Draft in DP2.0] With 4 emulated LTPR, Successful Link Training at all Supported Lane Counts and 8b10b Link 1 ✓
 - 7.1.3.6: [Draft in DP2.0] With 5 emulated LTPR, Successful Link Training at all Supported Lane Counts and 8b10b Link 1 ✓
 - 7.1.3.7: [Draft in DP2.0] With 6 emulated LTPR, Successful Link Training at all Supported Lane Counts and 8b10b Link 1 ✓
 - 7.1.3.8: [Draft in DP2.0] With 7 emulated LTPR, Successful Link Training at all Supported Lane Counts and 8b10b Link 1 ✓
- UHBR tests
 - 7.1.4.1: [Draft in DP2.0] With 0 emulated LTPR, Successful Link Training at all Supported Lane Counts and UHBR Link 1 ✓
 - 7.1.4.2: [Draft in DP2.0] With 1 emulated LTPR, Successful Link Training at all Supported Lane Counts and UHBR Link 1 ✓
 - 7.1.4.3: [Draft in DP2.0] With 2 emulated LTPR, Successful Link Training at all Supported Lane Counts and UHBR Link 1 ✓
 - 7.1.4.4: [Draft in DP2.0] With 3 emulated LTPR, Successful Link Training at all Supported Lane Counts and UHBR Link 1 ✓
 - 7.1.4.5: [Draft in DP2.0] With 4 emulated LTPR, Successful Link Training at all Supported Lane Counts and UHBR Link 1 ✓
 - 7.1.4.6: [Draft in DP2.0] With 5 emulated LTPR, Successful Link Training at all Supported Lane Counts and UHBR Link 1 ✓
 - 7.1.4.7: [Draft in DP2.0] With 6 emulated LTPR, Successful Link Training at all Supported Lane Counts and UHBR Link 1 ✓
 - 7.1.4.8: [Draft in DP2.0] With 7 emulated LTPR, Successful Link Training at all Supported Lane Counts and UHBR Link 1 ✓

DP 2.0 LTPR Device Compliance - Test Results

Compliance Test Results Viewer
DP 2.0 LTPR Device (Core R1.0) Compliance Test Results

HTML Report Instrument: MyM41h [10.30.196.186] CONTINUE TEST EXECUTION

Results Name: LTPR_Device_UHBR_UHBR
Date Tested: February 16, 2022 4:58 AM
Manufacturer: Model Name: Port Tested: 1

Overall Status: CTS Core R1.0 - Pass

- 7.1.3.8: [Draft in DP2.0] With 7 emulated LTPR, Successful Link Training at all Supported L 1 ✓
- 7.1.4.1: [Draft in DP2.0] With 0 emulated LTPR, Successful Link Training at all Supported L 1 ✓
- 7.1.4.2: [Draft in DP2.0] With 1 emulated LTPR, Successful Link Training at all Supported L 1 ✓
- 7.1.4.3: [Draft in DP2.0] With 2 emulated LTPR, Successful Link Training at all Supported L 1 ✓
- 7.1.4.4: [Draft in DP2.0] With 3 emulated LTPR, Successful Link Training at all Supported L 1 ✓
- 7.1.4.5: [Draft in DP2.0] With 4 emulated LTPR, Successful Link Training at all Supported L 1 ✓
- 7.1.4.6: [Draft in DP2.0] With 5 emulated LTPR, Successful Link Training at all Supported L 1 ✓
- 7.1.4.7: [Draft in DP2.0] With 6 emulated LTPR, Successful Link Training at all Supported L 1 ✓
- 7.1.4.8: [Draft in DP2.0] With 7 emulated LTPR, Successful Link Training at all Supported L 1 ✓

Iter 01:

- 01: [1] Link Training test for lane count = 1 and lane_rate = 10.00 PASS
- 02: [2] Link Training test for lane count = 2 and lane_rate = 10.00 PASS
- 03: [3] Link Training test for lane count = 4 and lane_rate = 10.00 PASS
- 04: [4] Link Training test for lane count = 2 and lane_rate = 13.50 PASS
- 05: [5] Link Training test for lane count = 2 and lane_rate = 13.50 PASS
- 06: [6] Link Training test for lane count = 4 and lane_rate = 13.50 PASS
- 07: [7] Link Training test for lane count = 1 and lane_rate = 20.00 PASS

Open ACA Data 07: [7] Link Training test for lane count = 1 and lane_rate = 20.00

DP Aux Channel Traces - From LTPR Test

ACA Data Viewer

Open Close Export Options Filter Find

[ACA_1_L_8_01] Events: 2674 (8239)

- 908 DMAT DPOBNC-R13 +00:32:37.803346 > R:50 FFC_CAPABILITY L=1
- 909 DMAT DPOBNC-R13 +00:32:37.803350 < ACK 8F
- 910 DMAT DPOBNC-R13 +00:32:37.803389 > R:60 DSC_SUPPORT L=16
- 911 DMAT DPOBNC-R13 +00:32:37.803363 < ACK 01 21 03 7F FB 07 01 00 0F 08 8E ...
- 912 DMAT DPOBNC-R13 +00:32:37.803375 > R:102 EDIP_CONFIGURATION_CAP L=1
- 913 DMAT DPOBNC-R13 +00:32:37.803449 < ACK 00
- 914 DMAT DPOBNC-R13 +00:32:37.803715 > R:701 EDIP_GENERAL_CAPABILITY L=1
- 915 DMAT DPOBNC-R13 +00:32:37.803793 < ACK 87
- 916 DMAT DPOBNC-R13 +00:32:37.804169 > R:102 EDIP_BACKGROUND_ABJ_CAPS L=1
- 917 DMAT DPOBNC-R13 +00:32:37.803936 < ACK 22
- 918 DMAT DPOBNC-R13 +00:32:37.804005 > R:725 EDIP_FEMUR_RPT_COUNT_MIN_L=1
- 919 DMAT DPOBNC-R13 +00:32:37.804079 < ACK 02 0C
- 920 DMAT DPOBNC-R13 +00:32:37.804169 > R:102 EDIP_REAL_CAPABILITIES L=1
- 921 DMAT DPOBNC-R13 +00:32:37.804237 < ACK 03
- 922 DMAT DPOBNC-R13 +00:32:37.804308 > R:114 RX_ALARM_CONFIGURATION L=1 01
- 923 DMAT DPOBNC-R13 +00:32:37.804390 < ACK
- 924 DMAT DPOBNC-R13 +00:32:37.804469 > R:1224 FEATURE_ENUMERATION_LIST_COUNT L=1
- 925 DMAT DPOBNC-R13 +00:32:37.804523 < ACK 01
- 926 DMAT DPOBNC-R13 +00:32:37.804603 > R:7 DOWN_STREAM_PORT_COUNT L=1
- 927 DMAT DPOBNC-R13 +00:32:37.804677 < ACK 41
- 928 DMAT DPOBNC-R13 +00:32:37.804745 > R:7 DOWN_STREAM_PORT_COUNT L=1
- 929 DMAT DPOBNC-R13 +00:32:37.804815 < ACK 41
- 930 DMAT DPOBNC-R13 +00:32:37.804802 > R:104 EDIP_CONFIGURATION_SET L=1 00
- 931 DMAT DPOBNC-R13 +00:32:37.805074 < ACK
- 932 DMAT DPOBNC-R13 +00:32:37.805043 > R:1202 FFC_CONFIGURATION L=1 01
- 933 DMAT DPOBNC-R13 +00:32:37.805125 < ACK
- 934 DMAT DPOBNC-R13 +00:32:37.805186 > R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
- 935 DMAT DPOBNC-R13 +00:32:37.805240 < ACK 00
- 936 DMAT DPOBNC-R13 +00:32:37.805430 > R:8 TRAINING_AUX_RD_INTERVAL L=1
- 937 DMAT DPOBNC-R13 +00:32:37.805204 < ACK 81
- 938 DMAT DPOBNC-R13 +00:32:37.805274 > R:102 EDIP_FIELD_DATA_STRUCTURE_SERV L=8
- 939 DMAT DPOBNC-R13 +00:32:37.805448 < ACK 20 18 03 04 10 01 07
- 940 DMAT DPOBNC-R13 +00:32:37.805800 > R:7003 PHY_REPEATER_MUOR L=1 AA
- 941 DMAT DPOBNC-R13 +00:32:37.805892 < ACK
- 942 DMAT DPOBNC-R13 +00:32:37.807750 > R:108 MAIN_LINE_CHANNEL_CODING_SET L=1 02
- 943 DMAT DPOBNC-R13 +00:32:37.807877 < ACK
- 944 DMAT DPOBNC-R13 +00:32:37.807935 > R:100 LINK_SW_SET L=1 04

Start Time: +00:32:37.865468
Bit Name Type Native
Direction: Reply
Command: ACK
Reply to Read Request.

FOODS: LTPR_FIELD_DATA_STRUCTURE_SERV Value Description
Bit Name Value Description
4-0 MAX_LANE_COUNT 0N Post Lanes
3-0 Minor Revision Number 0
7-4 Major Revision Number 2

FOODS: 8b10b_MAX_LANE_RATE_PHY_REPEATER Value Description
Bit Name Value Description
7-0 MAX_LANE_RATE 12b: 8.1 Gbps/Lane

FOODS: PHY_REPEATER_CNT Value Description
Bit Name Value Description
7-0 LTPR_COUNT 8th 8

FOODS: PHY_REPEATER_MUOR Value Description
Bit Name Value Description
7-0 Mode 5th: Transparent

FOODS: MAX_LANE_COUNT_PHY_REPEATER Value Description
Bit Name Value Description
4-0 MAX_LANE_COUNT 0N Post Lanes
6-0 Reserved 0 Reserved
7-0 Reserved 0 Reserved

FOODS: PHY_REPEATER_EXTENDED_MAX_TIMEOUT Value Description
Bit Name Value Description
6-0 EXT_MAX_TIMEOUT_REQUEST 16
7 EXT_MAX_TIMEOUT_RETRY 8(0)

FOODS: MAIN_LINE_CHANNEL_CODING_PHY_REPEATER Value Description
Bit Name Value Description
6-0 128b/132b_SUPPORTED Y(1)

939: < ACK 20 18 03 04 10 01 07

PANEL REPLAY FUNCTIONAL TESTING

Panel Replay Testing

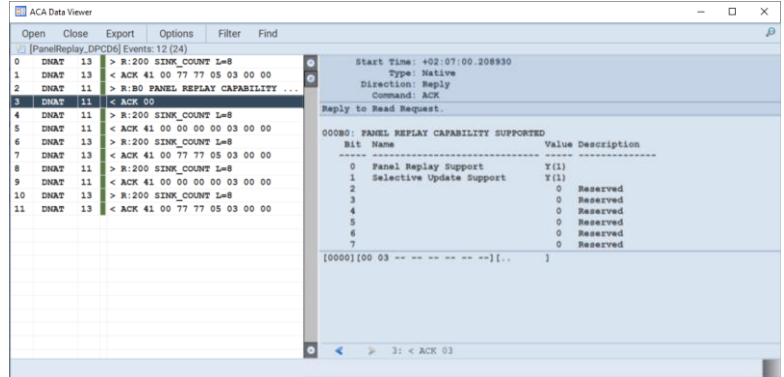
The M42d's supports functional testing of Panel Replay-capable source and display devices. The analysis support for testing sources provides emulation of a Panel Replay sink device. The Panel Replay sink functional test enables you to configure selected update regions through the command line (GUI implementation is future).

Panel Replay Source Analysis

The Real Time analyzer provides a real time update view (below) showing the incoming Panel Replay VSCs where you can see the changes from the previous frame. The transaction list (below right) shows the Panel Replay VSC metadata packets that have been sent with Selected Update regions. The panel on the right depicts the areas (blue box) where the selected transaction (left panel) VSCs and the SUs have indicated at change.

Panel Replay Aux Channel Monitor

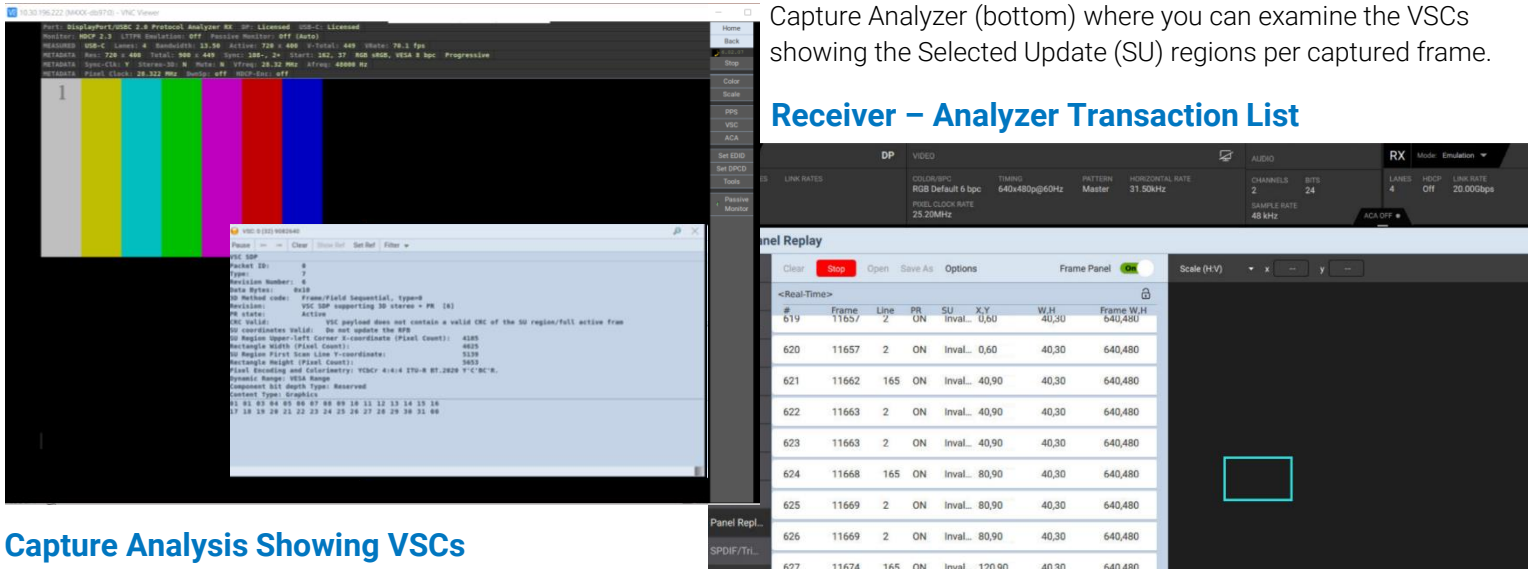
The M42d enables you to view the Aux transactions for discovery and configuration of Panel Replay (below).



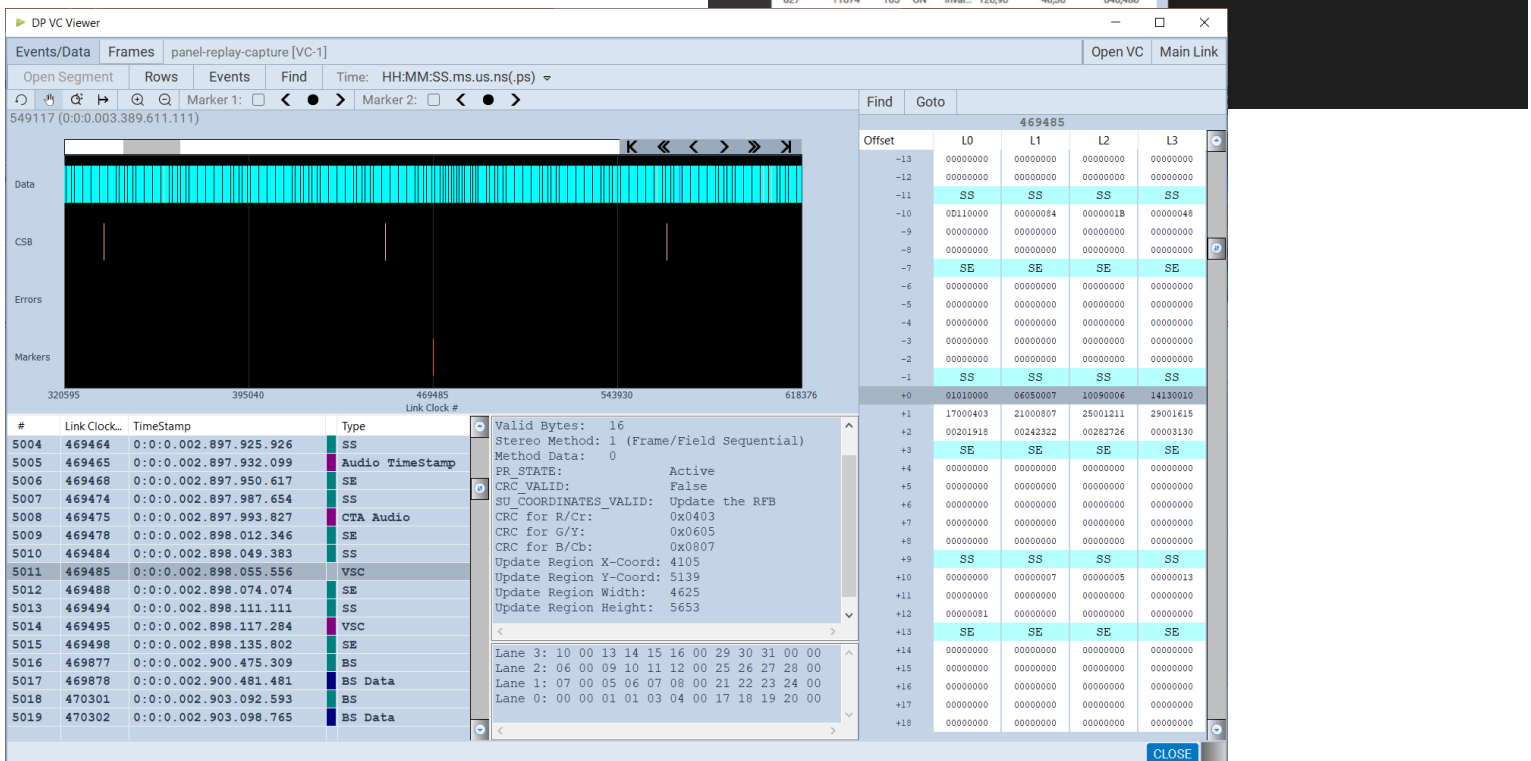
Capture Analysis

You can capture the Panel Replay VSC metadata packets in the Capture Analyzer (bottom) where you can examine the VSCs showing the Selected Update (SU) regions per captured frame.

Receiver - Analyzer Transaction List



Capture Analysis Showing VSCs



DisplayPort 2.0 Capabilities

Version	DisplayPort 2.0 (and DP 1.4)
Standard Video Formats	VESA, CTA
Protocols and Line Coding	DP, DSC, FEC, MST, SSC, SDP with 128b/132b encoding (LTTTPR, Panel Replay)
Video Data Rates	1.62, 2.7, 5.4, 8.1, 10.0, 13.5 & 20 Gb/s; 1, 2, 4 Lanes
Video Encoding / Color Depths	RGB, YCbCr - 8, 10, 12, 16 bits (6 bits future)
Video Sampling Modes	4:4:4, 4:2:2, 4:2:0
HDCP	Versions 1.3 and 2.3
Audio	8 Channel LPCM programmable sine wave
Capture memory	8 GBytes

Connectors - Front

DP Standard	Tx (1) DP Full-Sized; Rx (1) DP Full-Sized
USB-C	Tx (1) USB-C with DP Alt Mode; Rx (1) USB-C with DP Alt Mode
eDP Header	Pins to access eDP Tx backlight controls
USB (2)	For connecting keyboard and mouse for ATP Manager control & external storage media

Connectors – Back

HDMI - Admin Connector	HDMI 2.0 Port for external monitor for ATP Manager GUI
USB (2); USB-C (2)	Keyboard / mouse connected to USB ports to control ATP Manager on external display connected to Admin HDMI 2.0 port
RJ45 E1	For admin control over LAN from computer running ATP Manager
Cross Sync connector	Use for triggering a capture or for a capture event to trigger an oscilloscope (future)
All other connectors	Not used

Physical/Electric/Admin

Power	100-240 VAC, 50-60 Hz, 200 Watts
Size / Weight	Height: 3.44 in. (8.74 cm) Width: 9.57 in. (24.30 cm) Depth: 10.94 in. (27.79 cm) - 7.6 LBS; 5.057 Kg
Rack mountable	2 RU mounts in 19-inch rack with rack mounting brackets
Internal speaker	Speaker with volume control for monitoring incoming LPCM audio (future)
Command Line Control	Ethernet (RJ-45) for external GUI
System Control	External PC connected over LAN to Ethernet RJ45, VNC or Keyboard/mouse and 4K TV at Admin HDMI port
Environmental	Operating Temp: 32 to 104 (F); 0 to 40 (C)

Ordering/Product Code

Description

00-00259	M42d UHBR Video Analyzer/Generator (This is the Hardware System with basic video generation and analysis)
00-00261	M42d HBR3 Video Analyzer/Generator (This is the Hardware System with basic video generation and analysis)
95-00221	M42d Upgrade from HBR3 00-00261 System to UHBR rates with 00-00259 System
95-00222	Passive Probing Main Link and Aux Channel
95-00225	Sink Enhanced Functional test - Includes DSC, LTTTPR, Panel Replay & Adaptive Sync Functional Tests
95-00226	Source Enhanced Functional test – Includes DSC, Capture Analysis, LTTTPR, Panel Replay, Adaptive Sync Functional
95-00227	DP 1.4 Sink EDID/DisplayID compliance tests (requires 95-00225)
95-00228	DP 1.4 Source EDID/DisplayID compliance tests (requires 95-00226)
95-00232	DP 1.4/2.0 Source Link Layer & (MST future) compliance tests (DP 2.0 tests not fully supported; full suite future) (requires 95-00226)
95-00233	DP 1.4/2.0 Sink Link Layer & (MST future) compliance tests (Limited DP 2.0 tests currently supported; full suite future) (requires 95-00225)
95-00236	DP 1.4/2.0 DSC/FEC Source compliance tests (DP 2.0 tests are future) (requires 95-00226)
95-00237	DP 1.4/2.0 DSC/FEC Sink compliance tests (DP 2.0 tests are future) (requires 95-00225)
95-00240 NEW!	DP 1.4/2.0 LTTTPR Source compliance tests (requires 95-00226)
95-00241 NEW!	DP 1.4/2.0 LTTTPR Sink compliance tests (requires 95-00225)
95-00242 NEW!	DP 1.4/2.0 LTTTPR Device compliance tests (requires 95-00225 & 95-00226)
95-00234	DP 1.4/2.0 Adaptive Sync Source compliance test (support for DP 2.0 UHBR rates is future) (requires 95-00226)
95-00235	DP 1.4/2.0 Adaptive Sync Sink compliance test (support for DP 2.0 UHBR rates is future) (requires 95-00225)
95-00214	HDCP 2.3 Source compliance tests (requires 95-00226)
95-00217	HDCP 2.3 Sink compliance tests (requires 95-00225)
95-00212	Embedded DisplayPort (eDP) (Limited functions supported)
95-00209	M41x Rack-mount Kit





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