GREENTEST TECHNOLOGIES

PQSC
Programmable Quantum System Controller

Control of up to 100 qubits

Product Leaflet
Release date: August 2020

Key Features

- Synchronization of up to 18 HDAWGs: 144 AWG output channels with single-clock-cycle precision
- Low-latency feedback for qubit readout and successive control pulses
- Customization through user access to FPGA
- LabOne® control software with APIs for programming quantum algorithms

Summary

The Zurich Instruments PQSC Programmable Quantum System Controller brings together the instrumentation required for quantum computers with up to 100 qubits. Its ZSync low-latency, real-time communication links are designed specifically for quantum computing: the PQSC overcomes the practical limitations of traditional control methods, such as trigger lines or PXI buses, making rapid qubit calibration with perfect repeatable and phase-stable experiments a reality. Programming access to the powerful Xilinx UltraScale+ FPGA is the basis for developing new and optimized processing solutions for rapid tune-up and error correction adapted to the specific algorithm and computer architecture in use.

User Benefits

With the PQSC, users get access to state-of-the-art quantum information processing. Rapid tune-up procedures, syndrome decoding, and error correction routines are easily set up with the APIs. The PQSC guarantees a flexible system whose number of required AWG channels can be adapted to the needs of each application. It reduces complexity and required lab space. The time spent on AWG channel adjustment is minimal thanks to the sub-nanosecond synchronization of readout and control channels. This also holds true over reboot of the whole system thanks to the channel skew reproducibility. Altogether, the PQSC facilitates full flexibility and enables users to concentrate on the science of quantum computing while spending less time on implementation and system calibration.

Description

The PQSC features 18 ZSync ports to connect to the Zurich Instruments HDAWG Arbitrary Waveform Generator for qubit control. The latter is connected to the Zurich Instruments UHFQA Quantum Analyzer for qubit readout. In this master-slave configuration, the ZSync links distribute the system clock to all instruments and synchronize all instruments to sub-nanosecond levels. Small inter-AWG channel skews and minimal channel jitter can be adjusted in each AWG independently and remain constant over power cycles of the system. The PQSC functions as the central clock and central logic unit of the system, whereas the tasks for control and readout are distributed to the other instruments. A single-user interface controls and automatically synchronizes multiple instruments while providing status monitoring to ensure quality and reliability of qubit tune-up routines. Further, the ZSync links act as a bidirectional data interface to send qubit readout results to the PQSC for central processing, and to send the processing results to the slave instruments to enable synchronous actions. This division and distribution of tasks enables low-latency feedback for each individual readout and for successive control pulses. In addition, the ZSync links adhere to strict real-time behavior and all data transfers are predictable to single-clock-cycle precision. Lastly, the LabOne® control software provides a high-level interface to all instruments connected to the PQSC, and comes with APIs for Python, C, MATLAB®, LabVIEW® and .NET. With the APIs, quantum algorithms can be programmed at pulse and sample level; this guarantees an interface to higher programming languages at gate level and for data acquisition.

Specifications

General	
Dimensions	45 × 34.5 × 10 cm 17.7 × 13.6 × 3.9 inch
Weight	6.0 kg; 13.2 lbs
Power supply	AC: 100 - 240 V; 50 / 60 Hz

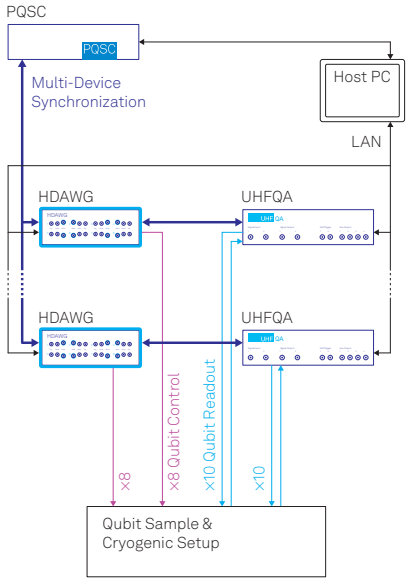
Connectivity	
Host connection	LAN/Ethernet: 1 Gbit/s, USB 3.0, JTAG over USB 2.0 for Xilinx® ChipScope™ access
Device connection	18 ZSync ports
ZSync communication bandwidth	Down-stream 200 MB/s, Up-stream 100 MB/s
ZSync communication latency	< 100 ns
Trigger	2 trigger inputs, 2 trigger outputs, 3.3 V TTL on SMA connector
Digital I/O	32 bits, 3.3 V TTL

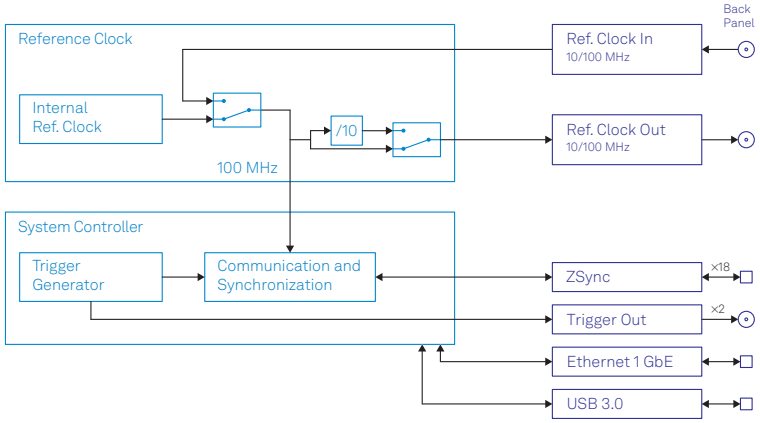
CPUs and memory	
Application processor	Quad ARM® Cortex TM-A53 up to 1,333 MHz
Real-time processor	Dual ARM® Cortex TM-R5 up to 533 MHz
SDRAM	4 GB DDR4 with ECC

FPGA characteristics	
Type	Xilinx® UltraScale+™ XCZU15EG-2I
System logic cells	747k
CLB flip-flops	682k
CLB LUTs	341k
DSP slices	3,528
Block RAM	26.2 Mb
Ultra RAM	31.5 Mb

Clock	
Input frequency	Auto-detect 10 MHz / 100 MHz
Input coupling	50 Ω, SMA connector
Output frequency	Switchable 10 MHz / 100 MHz
Output amplitude	>1 Vpp in 50 Ω

System synchronization characteristics	
Precision	Single clock cycle
Repetition rate	7 mHz (min) 10 MHz (max)
Hold-off time	100 ns (min) 143 s (max)
Jitter	ZSync CLK Output < 250 fs at 100 MHz





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广州总部：广州市番禺区陈边村金欧大道83号江潮创意园A栋208室
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南宁分公司：广西自由贸易试验区南宁片区五象大道401号五象航洋城1号楼3519号
广州分公司：广州市南沙区凤凰大道89号中国铁建·凤凰广场B栋1201房
电话：020-2204 2442
传真：020-8067 2851
邮箱：Sales@greentest.com.cn
官网：www.greentest.com.cn

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